WHAT IS CLAIMED IS:

1. A transistor, comprising:

an insulating substrate;

a first metal film disposed on the insulating substrate;

a first layer, which is arranged on the first metal film and which is made of an N-type semiconductor which is electrically coupled to the first metal film;

a second layer, which is disposed on the first layer and which is made of a P-type semiconductor;

a third layer, which is disposed on the second layer and which is made of an N-type semiconductor;

a second metal film, which is disposed on the insulating substrate in such a manner as not to be brought into contact with the first metal film, but which is brought into contact with the second layer; and

a third metal film which is disposed on the insulating substrate in such a manner as not to be brought into contact with the first metal film and the second metal film, but which is brought into contact with the third layer.

2. The transistor according to Claim 1,

the first layer being a collector,

the second layer being a base, and

the third layer being an emitter.

3. The transistor according to Claim 1,

the first metal film functioning as collector wiring,

the second metal film functioning as base wiring, and

the third metal film functioning as emitter wiring.

4. The transistor according to Claim 1,

the second layer being formed on an entire top surface of the first layer,

and the third layer is formed on a part of an area of the top surface of the second layer.

5. The transistor according to Claim 1,

the first layer and the second layer being each formed in a rectangular plate shape, and

the third layer being formed in a rectangular shape, which is longer and narrower than that of the first layer and the second layer.

6. The transistor according to Claim 1, the first layer, the second layer, and the third layer being formed so as to cross on a top surface of the first metal film.

7. The transistor according to Claim 1, the first layer, the second layer, and the third layer being formed of layers that are formed as tile-shaped elements, which are small tile-shaped semiconductor elements.

8. The transistor according to Claim 7, the tile-shaped elements being such that a collector electrode is formed on a bottom surface of the first layer, a base electrode is formed in an area other than the area where the third layer is provided on a top surface of the second layer, and an emitter electrode is formed on a top surface of the third layer, and

the collector electrode in the tile-shaped elements being joined to the first metal film, the base electrode being joined to the second metal film, and the emitter electrode being joined to the third metal film.

9. The transistor according to Claim 1, the transistor being formed of a transistor that functions as a hetero-bipolar transistor.

10. The transistor according to Claim 9,

the first layer being an N-type semiconductor made of gallium and arsenic,

the second layer is a P-type semiconductor made of gallium and arsenic, and

the third layer is an N-type semiconductor made of aluminum, gallium, and arsenic.

11. The transistor according to Claim 1,

a plurality of the first layers being provided on the one first metal film, and

the second layer and the third layer being provided for each of the first layers.

12. The transistor according to Claim 11,

a plurality of the second layers being coupled with one another by the one second metal film, and

a plurality of the third layers being coupled with one another by the one third metal film.

13. The transistor according to Claim 1, the first metal film, the second metal film, and the third metal film do not intersect one another.

14. The transistor according to Claim 1,

a portion of the second metal film that is not coupled to the second layer in the second metal film being directly provided on the insulating substrate, and

a portion of the third metal film that is not coupled to the third layer in the third metal film being directly provided on the insulating substrate.

15. An electronic device, comprising an optical interconnection circuit having the transistor according to Claim 1.